### SEMESTER I

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* The Term Work of Project stage II of semester IV should be assessed jointly by the pair of internal and external examiners along with the oral examination of the same.

**Note:** The Contact Hours for the calculation of load of teacher Seminar – 1Hr / week / student & Project – 2Hr / week / student

**Elective I:**
1. Fault Tolerant System Design
2. Advanced Digital System Design
3. Wireless and Mobile Technologies

**Elective II:**
1. Machine Intelligence
2. Advanced Computing Architectures
3. Memory Technologies

**Elective III:**
1. Digital Systems using PLDs
2. Biomedical Signals and Systems
3. Embedded Video processing

**Elective IV (OPEN):**
1. Reconfigurable Computing
2. Embedded Automotive Systems
3. Digital Signal Compression

Any one subject of Elective IV from the following branches
1. Computer Engineering
2. Information Technology
CMOS parasitics, technology scaling, CMOS Inverter, Voltage transfer Characteristics, Basic gates, W/L calculations, Static & dynamic power dissipations, PDP, Transmission gate, Applications of transmission gate, CMOS layout techniques, Subsystem design & layout, Domino logic, NORA logic, Transient response, Ultra fast VLSI ckt's & materials used. Mixed signal design issues, MOS switch, MOS diode/active resistor; current sinks, Current sources; Inverters, Cascode amplifier, Difference amplifier design. Data objects, data types, modeling methods, subprograms, packages, configuration, attributes, synthesizable & non-synthesizable statements, VITAL, VHDL codes for FSM, Processing elements, memory. Signal integrity issues, Floor planning methods, global routing, switch box routing, clock distribution, multiphase clock, off chip connections, I/O architectures, pad design, packages.

References
1. Management Perspectives
Role and importance of management, process of management – planning, organizing, staffing, directing, controlling. Nature, purpose and principles of management, Business policy, tools and techniques of strategic management, business ethics and social responsibilities

2. Preliminary planning of an IT Project
Gathering project Information, defining the project goals, establishing project priorities, requirements analysis, risk management, budgeting a project, creating a work breakdown structure, estimation

3. Organizing an IT Project
Organizing a Project Team: - Assessing internal scales, creating a team, managing team issues, resources procurement
Preparing and Implementing the project plan: - Defining the project schedule, project network diagram creation and analysis, project constraints, tracking project progress and financial obligations
Revising the project plan:-need for revision, establishing change control, implementing the project changes, coping with project delays

4. Group Dynamics and Team Management
Theories of Group Formation –Formal and Informal Groups and their interaction, Importance of teams - Formation of teams – Team Work, Leading the team, Team Meeting. Conflict Management - Traditional vis-à-vis Modern view of conflict, Conflict Process - Strategies for resolving destructive conflict, Stress management, employee welfare, energy management and energy audit,

5. Modern approaches to management
Concept of Knowledge management, change management, technology management, supply chain management, introduction to Intellectual property Rights (IPR)and cyber laws, process and project quality standards – six sigma, CMM, CMMI, PCMM, Impact of IT quality management systems, learning organizations

6. Applications of IT in management
Application of IT in functions like finance and accounting, stores, purchase, product design and development, quality control, logistics, customer relationship, marketing, project management, health care, insurance, banking, agriculture and service sector.
Reference Books:

2. Management-Tasks, Responsibilities and practices, Peter Drucker
3. Management Theory and Practice- Ernst Dale
4. Management Information System-Javadekar
5. Business Policy- Azhar Kazmi
Study of typical DSP algorithms: Convolution, Correlation, Digital filters: FIR and IIR filters, transforms: DFT, STFT, DCT, wavelets and filter banks, FFT algorithms and Implementation, general purpose hardware for signal processing facilities, Representations of the DSP algorithms, Pipelining and Parallel processing of FIR filters, Algorithm transformation: Retiming, Folding, Unfolding, Multirate Digital signal processing: Filters in sampling rate alteration systems, multistage design of decimator and interpolator, Arbitrary rate sampling rate converter, The polyphase decomposition, Digital filter banks, QMF filter banks, Multilevel filter banks. Basic building blocks of DSP systems: ALU, Multipliers, Dividers, Booth algorithm realizations, MAC, Barrel shifter, DSP processor architecture, Software developments, Selections of DSP processors, Implementation considerations, finite word length effects, real time implementation, Hardware interfacing, DSP processor architectures: TMS 320C54XX, TMS 320C67XX, Blackfin processor: Architecture overview, memory management, I/O management, On chip resources, programming considerations, Real time implementations, Applications of DSP systems Design using fixed point and floating point implementations: FIR filters, Multirate signal processing, IIR filters, DTMF generation and detection, FFT algorithms, wavelet algorithms, Inverse modeling.

Reference Books


504197  ELECTIVE I
FAULT TOLERANT SYSTEM DESIGN

Teaching Scheme
Lectures: 3 Hrs./Week

Examination Scheme
Theory: 100 Marks
Credit: 3


References
Digital System Design aspects for RISC and CISC CPU architectures, Control and Data path units of Processor, Practical design aspects for high frequency digital design such as clock skew and synchronous / asynchronous input signal handling. Hazard analysis, fault tree analysis. Estimation of digital system reliability. System integrity. Design of digital system for network applications such as ATM switch design, ATM packet generator, ATM packet decoder. Hardware testing and design for testability: Testing combinational and sequential logic, scan testing, boundary scan and BIST. VHDL models for memories and buses such as SRAM memory, 486 bus model and memory interfacing with microprocessor bus. Floating point arithmetic operations such as multiplications and others. Digital system design for asynchronous serial data transfer.

References


2. Charles H. Roth, “Digital system design using VHDL”, Thomson Publication


References


Adaptive Neuro-Fuzzy interface systems, Advanced Neuro-Fuzzy modeling,
Data clustering algorithms, Neuro-Fuzzy control, Fuzzy filtered neural network, Genetic algorithms in game playing.

References
Parallel Computer Models: The state of computing, Multiprocessors and multi-computers, Multivector and SIMD computers, Architectural development tracks

Program And Network Properties: Conditions of parallelism, Data and resource dependences, Hardware and software parallelism, Program partitioning and scheduling, Grain size and latency, Program flow mechanisms, Control flow versus data flow, Data flow architecture, Demand driven mechanisms, Comparisons of flow mechanisms


References

2. J. P. Hayes, “Computer Architecture And Organization”; MGH.
   Harvey G. Cragon, “Memory System and Pipelined Processors”; Narosa Publication.
3. V. Rajaranam & C.S.R.Murthy, “Parallel Computer”; PHI.
504198 ELECTIVE II
MEMORY TECHNOLOGIES

Teaching Scheme
Lectures: 3 Hrs./Week

Examination Scheme
Theory: 100 Marks
Credit: 3


References
The faculty associate with instruction of these subjects shall assign laboratory practices to the students, minimum three per course.

The laboratory practices shall encompass implementation/deployment of the course work in terms of the hardware setup, algorithm development and programming assignment. The student shall submit a document as a bonafide record of such assignment in the hard/soft copy format to the concerned faculty for further evaluation.
504201  EMBEDDED SYSTEMS

Teaching Scheme
Lectures: 3 Hrs./Week

Examination Scheme
Theory: 100 Marks
Credit: 3


References:
1. µC/OS-II, The Real Time Kernel, Jean J. Labrossy, Lawrence: R & D Publications.
4. ARM data books.
7.
504202 COMMUNICATION NETWORK AND SECURITY

Teaching Scheme

Lectures: 3 Hrs./Week

Examination Scheme

Theory: 100 Marks

Credit: 3


References

5. Evangelos Kranakis, “Primality and Cryptography”, John Wiley & Sons
504203  IMAGE PROCESSING AND PATTERN RECOGNITION

Teaching Scheme
Lectures: 3 Hrs./Week

Examination Scheme
Theory: 100 Marks
Credit: 3

Processing Images: Introduction, gray level sealing transformations, equalization, geometric image and interpolation, Smoothing, transformations, edge detection, Laplacian and sharpening operators, line detection and template matching, logarithmic gray level sealing, the statistical significance of image features.

Applications of pattern recognition, statistical decision theory, image processing and analysis.

Probability: Introduction, probability of events, random variables, Joint distributions and densities, moments of random variables, estimation of parameters from samples, minimum risk estimators

Statistical Decision Making: Introduction, Baye’s Theorem, multiple features, conditionally independent features, decision boundaries, unequal costs of error, estimation of error rates, the leaving—one—out technique. Characteristic curves, estimating the composition of populations.

Nonparametric Decision Making: Introduction, histograms, Kernel and window estimators, nearest neighbor classification techniques, adaptive decision boundaries, adaptive discriminate Functions, minimum squared error discriminate functions, choosing a decision making technique.

Clustering: Introduction, hierarchical clustering, partitional clustering Artificial Neural Networks, PCA, ICA, SVM,

Reference
2. Duda and Hart, “Pattern recognition (Pattern recognition a scene analysis)”
504204 ELECTIVE III
DIGITAL SYSTEMS USING PLDS

**Teaching Scheme**
Lectures: 3 Hrs./Week

**Examination Scheme**
Theory: 100 Marks
Credit: 3

Introduction to PLDs, ASIC, GPP, DSP processor, Features of PLDs, criteria for selection of PLD. Detailed study of state-of-art CPLD architectures (Xilinx XC9500 Series and Cool runner series/Altera). Detailed study of state-of-art FPGA architectures (Xilinx Spartan and Vertex Series/Altera). I/O interfacing. Compatibility with other logic families. Switch matrix/boxes design and related issues. PLD based system design with keyboard, LCD/LED display, ADC/DAC interfacing. PLD architectures for embedding soft cores. System Simulations using VHDL.

**References:**

1. Design warriors guide for FPGA, Elsevier Publication.
2. Data sheets of FPGA & CPLD

References

2. Eugene N Bruce, “Biomedical signal processing and signal modeling”, Wiley publications.
Digital video concepts, Subjective/Objective video quality measurement, Different standards for representing digital video, Need & types of video compression techniques, DPCM, Transform coding, DCT, DWT, Fast algorithms for the DCT, Implementation of DCT, Quantization, Entropy coding, Huffman coding, Arithmetic coding, Different video coding standards such as JPEG, Motion JPEG, JPEG 2000, MPEG(1,2,4), H.261, H.263, H.26L etc, Motion estimation and compensation requirements, Different methods, Comparison, Enhancements to the motion models, Software and Hardware implementations, Pre- & Post-processing, Bit rate and distortion, Computational complexity, Transmission of coded video, Design for optimum QoS, Transmission scenarios, Video codec interface, Design of a software and hardware CODEC, Design goals, Specifications, Designing the functional blocks and their testing. General purpose processors, DSP, Embedded processors, media processors, video signal processors, custom hardware, co-processors, any two real-life applications in details.

References

1. Iain E. G. Richardson, “Video Codec Design- Developing image and video compression systems”, WILEY Publication.
Computing requirements, Area, Technology scaling, Instructions, Custom Computing Machine, Overview, Comparison of Computing Machines. Interconnects, Requirements, Delays in VLSI Structures; Partitioning and Placement, Routing; Computing Elements, LUT’s, LUT Mapping, ALU and CLB’s, Retiming, Fine-grained & Coarse-grained structures; Multicontext; Comparison of different architectures viz. PDSPs, RALU, VLIW, Vector Processors, Memories, Arrays for fast computations, CPLDs, FPGAs, Multicontext, Partial Reconfigurable Devices; TSFPGA, DPGA, Matrix; Best suitable approach for RD; Case study. Control Logic, Binding Time and Programming Styles, Overheads, Data Density, Data BW, Function density, Function diversity, Interconnect methods, Best suitable methods for RD; Contexts, Context switching; Area calculations for PE; Efficiency, ISP, Hot Reconfiguration; Case study. Architectures for existing multi FPGA systems, Compilation Techniques for mapping applications described in a HDL to reconfigurable hardware, Study of existing reconfigurable computing systems to identify existing system limitations and to highlight opportunities for research; Software challenges in System on chip; Testability challenges; Case studies. Modelling, Temporal portioning algorithms, Online temporal placement, Device space management, Direct communication, Third party communication, Bus based communication, Ckt switching, Network on chip, Dynamic network on chip, Partial reconfigurable design.

References

2. IEEE Journal papers on Reconfigurable Architectures.

References:

References:

The faculty associate with instruction of these subjects shall assign laboratory practices to the students, minimum three per course.

The laboratory practices shall encompass implementation/deployment of the course work in terms of the hardware setup, algorithm development and programming assignment. The student shall submit a document as a bonafide record of such assignment in the hard/soft copy format to the concerned faculty for further evaluation.