COURSE STRUCTURE FOR M.E.(Electronics) (Digital System)
(w.e.f. June – 2008)

SEMESTER I

CODE	SUBJECT	TEACHING SCHEME		EXAMINATION SCHEME					CREDITS
		Lect.	Pr.	Paper	TW	Oral	Pr	Total	
504195	Microelectronics	3	-	100	-	-	-	100	3
504182	Principles and Practices for IT Management	3	-	100	-	-	-	100	3
504196	Signal Processing Architectures	3	-	100	-	-	-	100	3
504197	Elective I	3	-	100	-	-	-	100	3
504198	Elective II	3	-	100	-	-	-	100	3
504199	Digital System Design Practice I	-	6	-	50	-	-	50	3
504200	Seminar I	-	4	-	50	-	-	50	2
Total of First Term		15	10	500	100	-	-	600	20

SEMESTER II

CODE	SUBJECT	TEACHING SCHEME		EXAMINATION SCHEME					CREDITS
		Lect.	Pr.	Paper	TW	Oral	Pr	Total	
504201	Embedded Systems	3	-	100	-	-	-	100	3
504202	Communication Network and Security	3	-	100	-	-	-	100	3
504203	Image Processing and Pattern Recognition	3	-	100	-	-	-	100	3
504204	Elective III	3	-	100	-	-	-	100	3
504205	Elective IV (Open)	3	-	100	-	-	-	100	3
504206	Digital System Design Practice II	-	6	-	50	-	-	50	3
504207	Seminar II	-	4	-	50	-	-	50	2
Total of Second Term		15	10	500	100	-	-	600	20

SEMESTER III

CODE	SUBJECT	TEACHING SCHEME		EXAMINATION SCHEME					CREDITS
		Lect.	Pr.	Paper	TW	Oral	Pr	Total	
604184	Seminar III	-	4	-	50	-	-	50	2
604185	Project Stage I	-	18	-	50	-	-	50	6
Total of Third Term		-	22	-	100	-	-	100	8

SEMESTER IV

CODE	SUBJECT	TEACHING SCHEME		EXAMINATION SCHEME					CREDITS
		Lect.	**Pr.**	**Project**	**TW**	**Oral**	**Pr**	**Total**	
604186	Project Stage II	-	18		150*	50	-	200	12
Total of Fourth Term		-	18		150	50	-	200	12

* The Term Work of Project stage II of semester IV should be assessed jointly by the pair of internal and external examiners. along with the oral examination of the same.

Note: The Contact Hours for the calculation of load of teacher Seminar – 1Hr / week / student & Project – 2Hr / week / student

Elective I:

1. Fault Tolerant System Design
2. Advanced Digital System Design
3. Wireless and Mobile Technologies

Elective II:

1. Machine Intelligence
2. Advanced Computing Architectures
3. Memory Technologies

Elective III:

1. Digital Systems using PLDs
2. Biomedical Signals and Systems
3. Embedded Video processing

Elective IV (OPEN):

1. Reconfigurable Computing
2. Embedded Automotive Systems
3. Digital Signal Compression

Any one subject of Elective IV from the following branches

1. Computer Engineering
2. Information Technology

504195 MICROELECTRONICS

Teaching Scheme
Lectures: 3 Hrs./Week

Examination Scheme
Theory: 100 Marks
Credit: 3

CMOS parasitics, technology scaling, CMOS Inverter, Voltage transfer Characteristics, Basic gates, W/L calculations, Static & dynamic power dissipations, PDP, Transmission gate, Applications of transmission gate, CMOS layout techniques, Subsystem design & layout, Domino logic, NORA logic, Transient response, Ultra fast VLSI ckts & materials used. Mixed signal design issues, MOS switch, MOS diode/active resistor; current sinks, Current sources; Inverters, Cascode amplifier, Difference amplifier design. Data objects, data types, modeling methods, subprograms, packages, configuration, attributes, synthesizable & non-synthesizable statements, VITAL, VHDL codes for FSM, Processing elements, memory. Signal integrity issues, Floor planning methods, global routing, switch box routing, clock distribution, multiphase clock, off chip connections, I/O architectures, pad design, packages.

References

1. Allen and Holberg, “CMOS Analog Circuit Design”, Oxford Publication.
2. Pucknell and Kamran, “CMOS VLSI Design”, PHI Publication.
3. Perry, “VHDL”, TMH Publication.
4. Wayne Wolf, “Modern VLSI Design”, Pearson Publication.

504182 PRINCIPLES AND PRACTICES FOR IT MANAGEMENT

Teaching Scheme	Examination Scheme
Lectures: 3 Hrs./Week	Theory: 100 Marks
	Credit: 3

1. Management Perspectives

Role and importance of management, process of management – planning, organizing, staffing, directing, controlling. Nature, purpose and principles of management, Business policy, tools and techniques of strategic management, business ethics and social responsibilities

2. Preliminary planning of an IT Project

Gathering project Information, defining the project goals, establishing project priorities, requirements analysis, risk management, budgeting a project, creating a work breakdown structure, estimation

3. Organizing an IT Project

Organizing a Project Team: - Assessing internal scales, creating a team, managing team issues, resources procurement

Preparing and Implementing the project plan: - Defining the project schedule, project network diagram creation and analysis, project constraints, tracking project progress and financial obligations

Revising the project plan:-need for revision, establishing change control, implementing the project changes, coping with project delays

4. Group Dynamics and Team Management

Theories of Group Formation –Formal and Informal Groups and their interaction, Importance of teams - Formation of teams – Team Work, Leading the team, Team Meeting. Conflict Management - Traditional vis-à-vis Modern view of conflict, Conflict Process - Strategies for resolving destructive conflict, Stress management, employee welfare, energy management and energy audit,

5. Modern approaches to management

Concept of Knowledge management**,** change management, technology management, supply chain management, introduction to Intellectual property Rights (IPR)and cyber laws, process and project quality standards – six sigma, CMM, CMMI, PCMM, Impact of IT quality management systems, learning organizations

6. Applications of IT in management

Application of IT in functions like finance and accounting, stores, purchase, product design and development, quality control, logistics, customer relationship, marketing, project management, health care, insurance, banking, agriculture and service sector.

Reference Books:

1. Joseph Phillips, “IT Project Management”, Tata McGraw-Hill 2003 Edition
2. Management-Tasks, Responsibilities and practices, Peter Drucker
3. Management Theory and Practice- Ernst Dale
4. Management Information System-Javadekar
5. Business Policy- Azhar Kazmi
6. Industrial Energy Conservation- D.A.Ray, Pergamon Press
7. Resisting Intellectual Property-Halbert, Taylor & Francis Ltd ,2007

504196 SIGNAL PROCESSING ARCHITECTURES

Teaching Scheme	Examination Scheme
Lectures: 3 Hrs./Week	Theory: 100 Marks
	Credit: 3

Study of typical DSP algorithms: Convolution, Correlation, Digital filters: FIR and IIR filters, transforms: DFT, STFT, DCT, wavelets and filter banks, FFT algorithms and Implementation, general purpose hardware for signal processing facilities, Representations of the DSP algorithms, Pipelining and Parallel processing of FIR filters, Algorithm transformation: Retiming, Folding, Unfolding, Multirate Digital signal processing: Filters in sampling rate alteration systems, multistage design of decimator and interpolator, Arbitrary rate sampling rate converter, The polyphase decomposition, Digital filter banks, QMF filter banks, Multilevel filter banks. Basic building blocks of DSP systems: ALU, Multipliers, Dividers, Booth algorithm realizations, MAC, Barrel shifter, DSP processor architecture, Software developments, Selections of DSP processors, Implementation considerations, finite word length effects, real time implementation, Hardware interfacing, DSP processor architectures: TMS 320C54XX, TMS 320C67XX, Blackfin processor: Architecture overview, memory management, I/O management, On chip resources, programming considerations, Real time implementations, Applications of DSP systems Design using fixed point and floating point implementations: FIR filters, Multirate signal processing, IIR filters, DTMF generation and detection, FFT algorithms, wavelet algorithms, Inverse modeling.

Reference Books

1. K. K. Parhi, “VLSI Digital Signal Processing Systems- Design and Implementation”, John Wiley & Sons, Inc.
2. Sen M. Kuo and Woon-Seng Gan, “ Digital Signal Procesors, architectures, implementations, and applications”, Prentice-Hall, ISBN 0130352144.
3. Sanjit K. Mitra, “ Digital Signal Processing: A Computer based approach”, McCraw Hill, 1998, ISBN 070429537
4. Lawrence R. Rabiner and Bernard Gold, “ Theory and application of Digital signal Processing”, Prentice-Hall of India, 2006.
5. Madisetti, “ The Digital Signal Processing Handbook”, IEEE press, ISBN 0849385725

6. Vinay K. Ingale, John G. Proakis, 'Digital Signal Processing Using MATLAB", Thomson Publication.

504197 ELECTIVE I
FAULT TOLERANT SYSTEM DESIGN

Teaching Scheme	Examination Scheme
Lectures: 3 Hrs./Week	Theory: 100 Marks
	Credit: 3

Modeling: Basic Concept, Functional modeling at the logic level, Functional models at the register level, Structural models, Level of modeling. Type of simulation, unknown logic value, compiled simulation, Event-driven simulation and Hazard Detection. Logical fault models, Fault detection and redundancy, Fault equivalence and fault location, Fault Dominance, Single stuck-fault models, multiple stuck fault model, stuck RTL variables, Fault variables. Testing for Single Stuck fault and Bridging fault. General fault simulation techniques, Serial Fault simulation, Parallel fault simulation, Deductive fault simulation, Concurrent fault simulation, Fault simulation for combinational circuits, Fault sampling, Statistical fault analysis. General aspects of compression techniques, ones- count compression, transition – count compression, Parity – check compression, Syndrome testing and Signature Analysis Basic concepts, Multiple – Bit Errors, Checking circuits and self checking, self – checking checkers, Parity – check function, totally self-checking m/n code checkers, totally self-checking equality checkers, Self-checking Berger code checkers and self checking combinational circuits. Built In Self Test, Self-testing circuits for systems, memory & processor testing, PLA testing, Automatic test pattern generation and Boundary Scan Testing JTAG

References

1. M. Abramovici, M.A. Breuer, A.D. Friedman, "Digital systems testing and testable design", Jaico Publishing House.
2. Diraj K. Pradhan, "Fault Tolerant Computer System Design", Prentice Hall.

504197 ELECTIVE I

ADVANCED DIGITAL SYSTEM DESIGN

Teaching Scheme	Examination Scheme
Lectures: 3 Hrs./Week	Theory: 100 Marks
	Credit: 3

Digital System Design aspects for RISC and CISC CPU architectures, Control and Data path units of Processor, Practical design aspects for high frequency digital design such as clock skew and synchronous / asynchronous input signal handling. Hazard analysis, fault tree analysis. Estimation of digital system reliability. System integrity. Design of digital system for network applications such as ATM switch design, ATM packet generator, ATM packet decoder. Hardware testing and design for testability: Testing combinational and sequential logic, scan testing, boundary scan and BIST. VHDL models for memories and buses such as SRAM memory, 486 bus model and memory interfacing with microprocessor bus. Floating point arithmetic operations such as multiplications and others. Digital system design for asynchronous serial data transfer.

References

1. John F. Wakerly,"Digital Design principles and practices", 3rd edition, PHI publications
2. Charles H. Roth, "Digital system design using VHDL", Thomson Publication
3. Balabanian, "Digital Logic Design Principles", Wiley publication.
4. Stephen Brown, "Fundamentals of digital logic", TMH publication.

504197 ELECTIVE I
WIRELESS AND MOBILE TECHNOLOGIES

Teaching Scheme	Examination Scheme
Lectures: 3 Hrs./Week	Theory: 100 Marks
	Credit: 3

Wireless Communication Systems, Characteristics of radio propagation, Fading, Multipath propagation Mobile Networking: Mobile-IP, Ad-Hoc Networks and Ad-Hoc Routing, Wireless Protocols: Wireless TCP, Session Mobility, MAC protocols for digital cellular systems such as GSM. MAC protocols for wireless LANs such as IEEE802.11 and HIPERLAN I and II. The near far effect. Hidden and exposed terminals. Collision Avoidance (RTS-CTS) protocols. Mobile network layer protocols such as mobile-IP, Dynamic Host Configuration Protocol (DHCP). Mobile transport layer protocols such as mobile-TCP, indirect-TCP. Wireless Application Protocol (WAP). Mobile Agents, Transcending and Proxy Architecture, Wireless Web and WAP, Mobile Wireless Networks Simulation

References

1. T.S. Rappaport, Wireless communications; Principle and Practice, ISBN: 0-13-375536-3
2. J.Schiller, Mobile communications, ISBN: 0-321-12381-6, Addison-Wesley, 2003
3. A S. Tanenbaum, Computer Networks (Fourth Edition), Publisher: Prentice Hall PTR; ISBN: 0130661023; August, 2002
4. Dharjma Agrawal, An Zeng, " Introduction to Wireless and Mobile Systems", Thomson Publication.

504198 ELECTIVE II
MACHINE INTELLIGENCE

Teaching Scheme	Examination Scheme
Lectures: 3 Hrs./Week	Theory: 100 Marks
	Credit: 3

Introduction, Soft Computing intelligence, comparison with conventional Artificial Intelligence, soft computing characteristics, Fuzzy sets, Fuzzy rules and Fuzzy inference systems, Different fuzzy Models : Mamdani, Sugeno, Tsu Kamoto, Fuzzy modeling, Least squares methods for system identification, Derivative based optimization.

Neural networks, Adaptive networks, Supervised learning Neural networks, Perceptron, Backpropagation Multilayer perception, Radial basis function networks, Learning from reinforcement, Dynamic programming, Competitive learning, Kohonen's self organizing networks, Principle component networks, LVQ, Hopfield networks.

Adaptive Neuro-Fuzzy interface systems, Advanced Neuro-Fuzzy modeling,

Data clustering algorithms, Neuro-Fuzzy control, Fuzzy filtered neural network, Genetic algorithms in game playing.

References

1. S. R. Jang, C.T. Sun, E. Mizutani,' Neuro-Fuzzy and Soft Computing', Pearson Education, ISBN 81-297-0324-6.
2. B. Kosko, 'Neural Networks and Fuzzy Systems: a dynamical systems approach' Prentice Hall Publication.
3. Simon Haykin, ' Neural Networks: Comprehensive Foundation', Prentice Hall, ISBN-10: 0132733501.
4. Jacek M. Zurada , 'Introduction to Artificial Neural Systems', Jaico publications

504198 ELECTIVE II

ADVANCED COMPUTING ARCHITECTURES

Teaching Scheme	Examination Scheme
Lectures: 3 Hrs./Week	Theory: 100 Marks
	Credit: 3

Parallel Computer Models: The state of computing, Multiprocessors and multi-computers, Multi-vector and SIMD computers, Architectural development tracks

Program And Network Properties: Conditions of parallelism, Data and resource dependences, Hardware and software parallelism, Program partitioning and scheduling, Grain size and latency, Program flow mechanisms, Control flow versus data flow, Data flow architecture, Demand driven mechanisms, Comparisons of flow mechanisms

System Interconnect Architectures: Network properties and routing, Static interconnection networks, Dynamic interconnection Networks, Multiprocessor system interconnects, Hierarchical bus systems, Crossbar switch and multiport memory, Multistage and combining network. Processors and Memory Hierarchy: Advanced processor technology, Instruction-set Architectures, CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors, VLIW Architectures, Vector and Symbolic processors Memory Technology: Hierarchical memory technology, Inclusion, Coherence and Locality, Memory capacity planning, Virtual Memory Technology. Backplane Bus System: Backplane bus specification, Addressing and timing protocols, Arbitration transaction and interrupt, Cache addressing models, direct mapping and associative caches. Pipelining: Linear pipeline processor, Nonlinear pipeline processor, Instruction pipeline design, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch handling techniques, Arithmetic Pipeline Design, Computer arithmetic principles, Static arithmetic pipeline, Multifunctional arithmetic pipelines. Vector Processing Principles: Vector instruction types, Vector-access memory schemes. Synchronous Parallel Processing: SIMD Architecture and Programming Principles, SIMD Parallel Algorithms, SIMD Computers and Performance Enhancement

References

1. Kai Hwang, “Advanced Computer Architecture”; TMH.
2. J. P. Hayes, “Computer Architecture And Organization”; MGH.
   Harvey G. Cragon, “Memory System and Pipelined Processors”; Narosa Publication.
3. V. Rajaranam & C.S.R.Murthy, “Parallel Computer”; PHI.
4. R. K. Ghose, Rajan Moona & Phalguni Gupta, “Foundation of Parallel Processing”; Narosa Publications. Kai Hwang and Zu, “Scalable Parallel Computers Architecture”; MGH.

504198 ELECTIVE II
MEMORY TECHNOLOGIES

Teaching Scheme	Examination Scheme
Lectures: 3 Hrs./Week	Theory: 100 Marks
	Credit: 3

Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, SOl, Advanced SRAM Architectures, Application Specific SRAMs; DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAM, High Density ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Nonvolatile SRAM, Flash Memories. RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing. General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Reliability Modeling and Failure Rate Prediction, Reliability Screening and Qualification. Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing, Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices. Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging, Future Directions, Introduction to digital tablet PC, LCD, DVD player etc.

References

1. Ashok K.Sharma, " Semiconductor Memories Technology, Testing and Reliability ", Prentice-Hall of India Private Limited, New Delhi, 1997.
2. “Memories”, Springer Publication.
3. Wen C. Lin, “Handbook of Digital System Design”, CRC Press.

504199 DIGITAL SYSTEM DESIGN PRACTICE I

Teaching Scheme	Examination Scheme
Practical: 6 Hrs./Week	**TW: 50 Marks**

The faculty associate with instruction of these subjects shall assign laboratory practices to the students, minimum three per course.

The laboratory practices shall encompass implementation/ deployment of the course work in terms of the hardware setup, algorithm development and programming assignment. The student shall submit a document as a bonafide record of such assignment in the hard/soft copy format to the concerned faculty for further evaluation.

504201 EMBEDDED SYSTEMS

Teaching Scheme	Examination Scheme
Lectures: 3 Hrs./Week	Theory: 100 Marks
	Credit: 3

Digital Systems and Embedded Systems, Design Methodology, Design Metrics, Specialties. Integrated Circuits Technologies- Full custom/VLSI, Logic Families, ASICs, PLD, PAL, CPLDs, FPGA, Packaging and Circuit Boards, Interconnection and Signal Integrity, Differential Signaling. General Purpose Processor, System On chip. RISC Processor Architecture: Embedded Computer Organization, ARM 7/ARM 9 architecture: Microcontrollers and Processor Cores, Instructions and Data handling, interfacing with Memory, Interrupts, Timers, ARM Bus. I/O Devices, I/O Controllers, Simple & Autonomous I/O Controllers, Parallel, Multiplexed, Tristate, and Open-Drain Buses, Bus Protocols, Serial Transmission Techniques &standards, Wireless protocols, CAN & advanced Buses, I/O Software. Embedded Software: Software Architectures, Software Developments Tools, Programming Concepts, Embedded Programming in C and C++, Queues, Stacks, Optimization of Memory needs, Program Modeling Concepts, Software Development Process Life Cycle and its Model, Software Analysis, Design and Maintenance. Real Time Operating Systems (µC/OS): Real Time Software Concepts, Kernel Structure, Task Management, Time Management, Inter task Communication & Synchronization, Memory Management, and Porting µCos-II.

References:

1. µC/OS-II, The Real Time Kernel, Jean J. Labrossy, Lawrence: R & D Publications.
2. Embedded Real Time Systems: Concepts, Design & Programming, Dr. K.V.K.K. Prasad, Dreamtech Publication.
3. Embedded System Design: A unified Hardware/Software Introduction, Frank Vahid, and Tony Givargis, Wiley Publication.
4. ARM data books.
5. An Embedded Software Primer, David E. Simon, Pearson Education Publication.
6. Embedded Systems Architecture, Programming and design, Raj Kamal, Tata MCgraw-Hill Publication.
7.

504202 COMMUNICATION NETWORK AND SECURITY

Teaching Scheme	Examination Scheme
Lectures: 3 Hrs./Week	Theory: 100 Marks
	Credit: 3

Network and Transport Layers: Mobile IP, TCP: Traditional, Indirect, Snooping, Mobile, TCP/IP protocol stack over IEEE 802.11b, wireless adaptation layer (WAL), ATM, Frame Relay, IEEE 802.11 WLANs analysis, deployment of 802.11 infrastructure; Bluetooth, core protocols, MANETs and WSNs. Mobile Ad Hoc networks: MAC Protocols - classification, comparative analysis, reactive and proactive routing, power-aware routing, performance comparison; Quality of Service. Wireless Sensor Networks: Data Dissemination, Data Gathering, MAC Protocols, Sensor Management, Localization. Conventional encryption, cipher-block, location of encryption devices, key distribution. Public key cryptography, RSA algorithm, diffie-hellman algorithms, message authentication, secure hash functions, HMAC, digital signatures, key management. Secrete Key Cryptography, DES, IDEA, AES. Network Security applications: Authentication applications email Security, PGP, SMIME IP Security, authentication on header, encapsulating security payload, combining security associations, key management. Web Security Requirements, SSL and TSL, SET

References

1. C. Siva Ram Murthy and B. S. Manoj, “Ad Hoc Wireless Networks: Architectures and Protocols”, Prentice Hall.
2. Jochen Schiller, “Mobile Communications”, Addison Wesley, 2000.
3. Ramjee Prasad and Luis Munoz, “WLANs and WPANs towards 4G wireless”, Artech House, 2003.
4. William Stallings, “ Cryptography and Network Security”, 3rd edition, Pearson Education
5. Evangelos Kranakis, “ Primality and Cryptography”, John Wiley & Sons
6. Rainer A. Ruppel, “ Analysis and Design of Stream Ciphers”, Springer Verlag
7. Douglas A. Stinson, “Cryptography, Theory and Practice”, 2nd edition, Chapman & Hall, CRC Press Company, Washington

504203 IMAGE PROCESSING AND PATTERN RECOGNITION

Teaching Scheme	Examination Scheme
Lectures: 3 Hrs./Week	Theory: 100 Marks
	Credit: 3

Processing Images: Introduction, gray level sealing transformations, equalization, geometric image and interpolation, Smoothing, transformations, edge detection, Laplacian and sharpening operators, line detection and template matching, logarithmic gray level sealing, the statistical significance of image features.

Applications of pattern recognition, statistical decision theory, image processing and analysis. Probability: Introduction, probability of events, random variables, Joint distributions and densities, moments of random variables, estimation of parameters from samples, minimum risk estimators Statistical Decision Making: Introduction, Baye's Theorem, multiple features, conditionally independent features, decision boundaries, unequal costs of error, estimation of error rates, the leaving-one—out technique. Characteristic curves, estimating the composition of populations. Nonparametric Decision Making: Introduction, histograms, Kernel and window estimators, nearest neighbor classification techniques, adaptive decision boundaries, adaptive discriminate Functions, minimum squared error discriminate functions, choosing a decision making technique. Clustering: Introduction, hierarchical clustering, partitional clustering Artificial Neural Networks, PCA, ICA, SVM,

Reference

1. Eart Gose, Richard Johnsonburg and Steve Joust, "Pattern Recognition and Image Analysis", Prentice-Hall of India-2003.
2. Duda and Hart, "Pattern recognition (Pattern recognition a scene analysis)"
3. Robert J Schalkoff, "Pattern recognition : Statistical ,Structural and neural approaches", John Wiley
4. Milan Sonka Vaclav Hlavac Roger Boyle,"Image Processing, Analysis, and Machine Vision",Second Edition, Thomson Publication
5. Rafel Gonzallez and R. Woods," Digital Image Processing", Second edition,

504204 ELECTIVE III

DIGITAL SYSTEMS USING PLDS

Teaching Scheme	Examination Scheme
Lectures: 3 Hrs./Week	Theory: 100 Marks
	Credit: 3

Introduction to PLDs, ASIC, GPP, DSP processor, Features of PLDs, criteria for selection of PLD. Detailed study of state-of-art CPLD architectures (Xilinx XC9500 Series and Cool runner series/Altera). Detailed study of state-of-art FPGA architectures (Xilinx Spartan and Vertex Series/Altera). I/O interfacing. Compatibility with other logic families. Switch matrix/ boxes design and related issues. PLD based system design with keyboard, LCD/LED display, ADC/DAC interfacing. PLD architectures for embedding soft cores. System Simulations using VHDL.

References:

1. Design warriors guide for FPGA, Elsvier Publication.
2. Data sheets of FPGA & CPLD

504204 ELECTIVE III

BIOMEDICAL SIGNALS AND SYSTEMS

Teaching Scheme
Lectures: 3 Hrs./Week

Examination Scheme
Theory: 100 Marks
Credit: 3

Introduction to Biomedical Signals,Nature of Biomedical Signals, Examples of Biomedical Signals –EMG, ECG, EEG, ERPs,PCG,VMG, VAG, Objectives of Biomedical Signal Analysis, Difficulties in Biomedical Signal Analysis, Concurrent, Coupled, and Correlated Processes-Illustration of the Problem with Case-Studies. Filtering for Removal of Artifacts- Illustration of the Problem with Case-Studies,Time-Domain Filters, Frequency-Domain Filters, Optimal Filtering, The Wiener Filter, Adaptive Filters for Removal of Interference, Selecting an Appropriate Filter Application: Removal of Artifacts in the ECG, Event Detection, Detection of Events and Waves, Correlation Analysis of EEG channels, Cross-spectral Techniques. The Matched Filter, Detection of the P Wave, Homomorphic Filtering, Application- ECG Rhythm Analysis, Identification of Heart Sounds, Waveshape and waveform Complexity, Analysis of Event-related Potentials, Morphological Analysis of ECG Waves, Envelope Extraction and Analysis of Activity, Application- Normal and Ectopic ECG Beats, Analysis of Exercise ECG. Frequency-domain Characterization The Fourier Spectrum, Estimation of the Power Spectral Density Function, Measures Derived form PSDs. Modeling Biomedical Systems, Point Processes Parametric System Modeling Autoregressive of All-pole Modeling, Pole-Zero Modeling, Electromechanical Models of Signal Generation, Application-Heart-rate Variability, Spectral Modeling and Analysis of PCG. Analysis of Nonstationary Signals, Time-Variant Systems, Fixed Segmentation, Adaptive Segmentation, Use of Adaptive Filters for Segmentation, Application- Adaptive Segmentation of EEG Signals, Adaptive Segmentation of PCG Signals. Pattern Classification and Diagnostic Decision , Pattern Classification, Supervised Pattern Classification, Unsupervised Pattern Classification, Probabilistic Models and Statistical Decision , Logistic regression Analysis The Training and Test Steps, Neural Networks, Measures of Diagnostic Accuracy and Cost, Reliability of Classifier and Decisions

References

1. R. M. Rangayyan “Biomedical Signal Analysis- A case study approach”, Wiley Publications.
2. Eugene N Bruce, “Biomedical signal processing and signal modeling”, Wiley publications.

504204 ELECTIVE III
EMBEDDED VIDEO PROCESSING

Teaching Scheme
Lectures: 3 Hrs./Week

Examination Scheme
Theory: 100 Marks
Credit: 3

Digital video concepts, Subjective/Objective video quality measurement, Different standards for representing digital video ,Need & types of video compression techniques,DPCM,Transform coding ,DCT, DWT, Fast algorithms for the DCT, Implementation of DCT, Quantization, Entropy coding, , Huffman coding, Arithmetic coding, Different video coding standards such as JPEG, Motion JPEG, JPEG 2000,MPEG(1,2,4),H.261,H.263,H.26L etc, Motion estimation and compensation requirements, Different methods, Comparison, Enhancements to the motion models, Software and Hardware implementations, Pre- & Post-processing, Bit rate and distortion, Computational complexity, Transmission of coded video, Design for optimum QoS , Transmission scenarios,Video codec interface, Design of a software and hardware CODEC, Design goals, Specifications, Designing the functional blocks and their testing. General purpose processors, DSP, Embedded processors, media processors, video signal signal processors, custom hardware, co-processors, any two real –life applications in details.

References

1. Iain E. G. Richardson, “Video Codec Design- Developing image and video compression systems”, WILEY Publication.
2. Vasudev Bhaskaran, Konstantinos Konstantinides, “Image and video compression standards”, Kluwer academic publishers

504205 ELECTIVE IV (OPEN)
RECONFIGURABLE COMPUTING

Teaching Scheme	Examination Scheme
Lectures: 3 Hrs./Week	Theory: 100 Marks
	Credit: 3

Computing requirements, Area, Technology scaling, Instructions, Custom Computing Machine, Overview, Comparison of Computing Machines. Interconnects, Requirements, Delays in VLSI Structures; Partitioning and Placement, Routing; Computing Elements, LUT's, LUT Mapping, ALU and CLB's, Retiming, Fine-grained & Coarse-grained structures; Multicontext; Comparison of different architectures viz. PDSPs, RALU, VLIW, Vector Processors, Memories, Arrays for fast computations, CPLDs, FPGAs, Multicontext, Partial Reconfigurable Devices; TSFPGA, DPGA, Mattrix; Best suitable approach for RD; Case study. Control Logic, Binding Time and Programming Styles, Overheads, Data Density, Data BW, Function density, Function diversity, Interconnect methods, Best suitable methods for RD; Contexts, Context switching; Area calculations for PE; Efficiency, ISP, Hot Reconfiguration; Case study. Architectures for existing multi FPGA systems, Compilation Techniques for mapping applications described in a HDL to reconfigurable hardware, Study of existing reconfigurable computing systems to identify existing system limitations and to highlight opportunities for research; Software challenges in System on chip; Testability challenges; Case studies. Modelling , Temporal portioning algorithms, Online temporal placement, Device space management, Direct communication, Third party communication, Bus based communication, Ckt switching, Network on chip, Dynamic network on chip, Partial reconfigurable design.

References

1. Andre Dehon, "Reconfigurable Architectures for General Purpose Computing", MIT Publication.
2. IEEE Journal papers on Reconfigurable Architectures..
3. "High Performance Computing Architectures" (HPCA) Society papers.
4. Christophe Bobda, "Introduction to Reconfigurable Computing", Springer Publication.
5. .Maya Gokhale, Paul Ghaham, "Reconfigurable Computing", Springer Publication.

504205 ELECTIVE IV (OPEN)
EMBEDDED AUTOMOTIVE SYSTEMS

Teaching Scheme	Examination Scheme
Lectures: 3 Hrs./Week	Theory: 100 Marks
	Credit: 3

Current trends in Automobiles, open loop and closed loop systems - components for electronic engine management system. Electro magnetic interference suppression. Electromagnetic compatibility, Electronic dashboard instruments, onboard diagnostic system , security and warming system. Electronic management of chassis systems. Vehicle motion control. Sensors and actuators, and their interfacing. Basic sensor arrangement, types of sensors such as- oxygen sensors, crank angle position sensors- Fuel metering/ vehicle speed sensors and destination sensors, Attitude sensor, Flow sensor, exhaust temperature, air mass flow sensors. Throttle position sensor, solenoids, stepper motors, relays. Electronic ignition systems. Types of solid state ignition systems and their principle of operation. Digital engine control system. Open loop and closed loop control system, Engine cranking and warm up control. Acceleration enrichment. Deceleration learning and ideal speed control, Distributor less ignition – Integrated engine control system, Exhaust emission control engineering. Automotive Embedded systems. PIC, Freescale microcontroller based system. Recent advances like GLS,GPSS,GMS. Multiprocessor communication using CAN bus. Case study- cruise control of car. Artificial Intelligence and engine management.

References:

1. William B. Riddens, “Understanding Automotive Electronics”, 5th Edition, Butterworth Hennimann Woburn, 1998.
2. Young A.P. & Griffiths, “ Automotive Electrical Equipment” , ELBS & New Press-1999.
3. Tom Weather Jr. & Cland c. Ilunter, “ Automotive computers and control system” , Prentice Hall Inc., New Jersey.
4. Crouse W.H., “ Automobile Electrical Equipment” , Mc Graw Hill Co. Inc., New York ,1995.
5. Bechhold, “ Understanding Automotive Electronic”, SAE,1998.
6. Robert Bosch,” Automotive Hand Book”, SAE (5TH Edition),2000.

504205 ELECTIVE IV (OPEN)
DIGITAL SIGNAL COMPRESSION

Teaching Scheme
Lectures: 3 Hrs./Week

Examination Scheme
Theory: 100 Marks
Credit: 3

Lossless vs. Lossy, Example Motivating Lossless, Math Preliminaries for Lossless Methods, Huffman & Aritmetic coding, Audio compression: Modelling sound, Sampling, Nyquist, Quantisation-Scalar quantisation,Uniform quantisers, Non-uniform quantisers. Compression performance, Speech compression-Speech coders,Predictive approaches,Silence compression,Pulse code modulation (ADPCM),Music compression,Streaming audio, MIDI . Math Preliminaries for Lossy Methods :Random Processes and Their Models, Distortion Criteria/Measures, Info Theory for Lossy, Rate-Distortion Theory . Quantization- Optimal and Adaptive Quantization, Uniform and nonuniform Quantizers, Entropy Coded, Vector Math for Transforms, Subbands, and Wavelets : Matrices and Vectors, Eigenvectors Coding : Transform coding Subband Coding- Intro and Multirate, Subband, Perfect Recon Filters. Wavelet Compression Methods :2-D Wavelet for Image Compression, choice of wavelet for image compression, Embedded Image Coding Using Zerotrees, EZW charts, SPIHT Charts.Video compression: Analogue video, Digital video, Moving pictures, MPEG, Basic principles, Temporal compression algorithms, Group of pictures, Motion estimation, Work in different video formats.

References:

1. Jayanth N S and Noll P, "Digital Coding of Waveforms - Principles and Application to Speech and Video," Prentice Hall, 1984.
2. Kondoz A M, "Digital Speech," John Wiley, 1994.
3. Gersho A and Gray R, "Vector Quantization and Signal Compression," Kluwer Acad Publication, 1992.
4. Hanzo L, Somernille F C A, Woodard J P, "Voice Compression and Communications," John Wiley, 2001
5. Yun Q. Shi, Huifang Sun "Image and Video Compression for Multimedia Engineering: Fundamentals, Algorithms, and Standards"CRC press
6. Ida Mengyi Pu, “Fundamental Data Compression”, Elsevier Publications

504206 DIGITAL SYSTEM DESIGN PRACTICE II

Teaching Scheme	Examination Scheme
Practical: 6 Hrs./Week	TW: 50 Marks

The faculty associate with instruction of these subjects shall assign laboratory practices to the students, minimum three per course.

The laboratory practices shall encompass implementation/ deployment of the course work in terms of the hardware setup, algorithm development and programming assignment. The student shall submit a document as a bonafide record of such assignment in the hard/soft copy format to the concerned faculty for further evaluation.